

Size:  
1.91 x 1.09 x 0.37 in  
48,6 x 27,7 x 9,5 mm

## Features

- -55°C to 100°C baseplate operation
- Isolated 1 to 50 Vout
- High density
- Small footprint
- ZVS / ZCS Sine Amplitude Converter
- 3 MHz effective switching frequency
- Low weight – 1.10 oz (31.3 g)
- 1  $\mu$ s transient response
- Up to 96.5% efficiency

## Product Overview

The VI BRICK VTM Current Multiplier provides extremely fast, efficient, and quiet fixed ratio voltage division (or current multiplication). With twelve voltage division ratios from 1:1 to 1:32, the isolated VI BRICK VTM provides the user with the flexibility to supply up to 100 A or 120 W at any output voltage from 1 to 50 Vdc in a package occupying ~ 2 square inches.

The Military COTS VI BRICK VTMs are optimized for use with the Military Pre-Regulator Module to implement a Factorized Power Architecture (FPA).

Together, the PRM™ + VTM set provides the full functionality of a DC-DC converter, but with breakthrough performance and flexibility in a rugged, miniature package. The companion VI BRICK PRM for the MT036 family of VI BRICK VTMs is the 28 Vdc input MR028A036M012FP, which operates from an input range of 16-50 Vdc (the data sheet is available at vicorpower.com). The VTM can also be used as a standalone POL product.

By factorizing the DC-DC power conversion into its essential elements – isolation and transformation on the one hand, and the

output voltage control and regulation on the other – and arranging those functions in a sequence that maximizes system performance, FPA offers a fundamentally new and significantly improved approach to power conversion.

The VI BRICK VTM's fast dynamic response and low noise eliminate the need for bulk capacitance at the load, substantially increasing the POL density while improving reliability and decreasing cost.

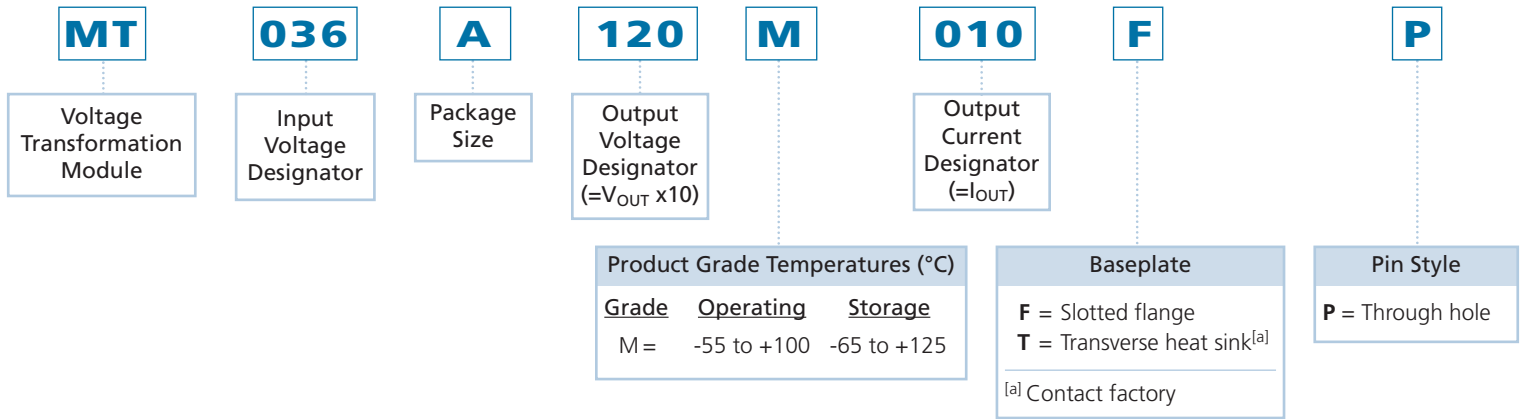
## Absolute Maximum Ratings

Parameter	Values	Unit	Notes
+In to -In	-1.0 to 60	Vdc	
+In to -In	100	Vdc	For 100 ms
PC to -In	-0.3 to 7.0	Vdc	
VC to -In	-0.3 to 19.0	Vdc	
+Out to -Out	Model specific	Vdc	
Isolation voltage	2,250	Vdc	Input to output
Output current	Model specific	A	Continuous
Peak output current	1.5 • Iout	A	For 1 ms
Output power	120	W	Continuous
Peak output power	180	W	For 1 ms
Operating temperature	-55 to +100	°C	M-Grade; baseplate
Storage temperature	-65 to +125	°C	M-Grade

**Note:** Stresses in excess of the maximum ratings can cause permanent damage to the device. Operation of the device is not implied at these or any other conditions in excess of those given in the specification. Exposure to absolute maximum ratings can adversely affect device reliability.

# SPECIFICATIONS

## PART NUMBERING



### Input Specifications *(Conditions are at 36 Vin, full load, and 25°C baseplate unless otherwise specified)*

Parameter	Min	Typ	Max	Unit	Notes
Input voltage range	26	36	50	Vdc	Operable down to zero V with VC voltage applied
Input dV/dt			1	V/ $\mu\text{s}$	
Input overvoltage turn-on	50.5	54.5		Vdc	
Input overvoltage turn-off		55.5	57.5	Vdc	
Input current			3.5	Adc	Continuous
No load power dissipation	1.5	3.0	6.0	W	Low line to high line

### Output Specifications *(Conditions are at 36 Vin, full load, and 25°C baseplate unless otherwise specified)*

Parameter	Min	Typ	Max	Unit	Note
Output voltage	See Table 1			Vdc	No load
	$K \cdot V_{IN} - I_O \cdot R_{OUT\ NOM}$			Vdc	Full load
Rated DC current	0		100	Adc	26 – 50 $V_{IN}$ See Table 1, Page 5
Peak repetitive current			150%	$I_{MAX}(A)$	Max pulse width 1ms, max duty cycle 10%, baseline power 50%
DC current limit		160%		$I_{NOM}(A)$	Module will shut down when current limit is reached or exceeded
Short circuit protection set point	47.4			Adc	Module will shut down
Current share accuracy		5	10	%	See Parallel Operation on Page 8
Efficiency					See Table 2, Page 5
Load capacitance					See Table 2 when used with PRM
Output overvoltage setpoint		110%	115%	$V_{OUT\ MAX}$	
Output ripple voltage (Typ)					
No external bypass	50		250	mV	See Figures 2 and 5
10 $\mu\text{F}$ bypass capacitor	2		20	mV	See Figure 6
Effective switching frequency	2.5	3.0	3.6	MHz	Model dependent
Line regulation	0.99K	K	101K		$V_{OUT} = K \cdot V_{IN}$ at no load, See Table 1
Load regulation	$R_{OUT\ MIN}$		$R_{OUT\ MAX}$	$\text{m}\Omega$	See Table 1
Transient response					
Response time		200		ns	See Figures 7 and 8
Recovery time		1		$\mu\text{s}$	See Figures 7 and 8

TYPICAL WAVEFORMS & PLOTS

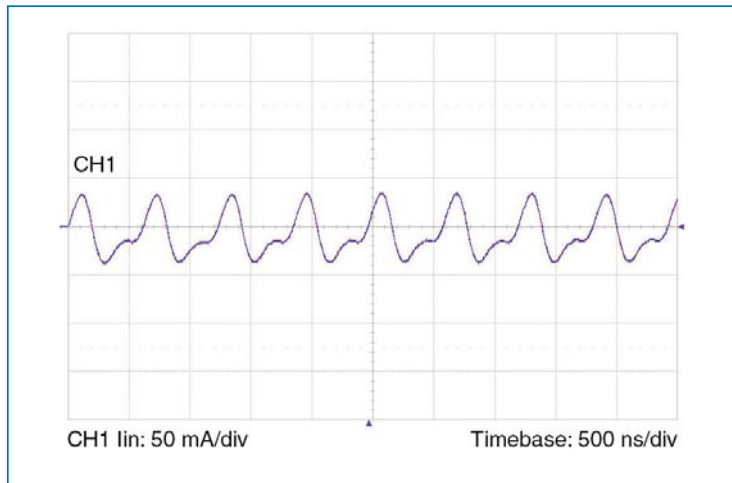


Figure 1 — Representative input reflected ripple current at full load (MT036A120M010FP)

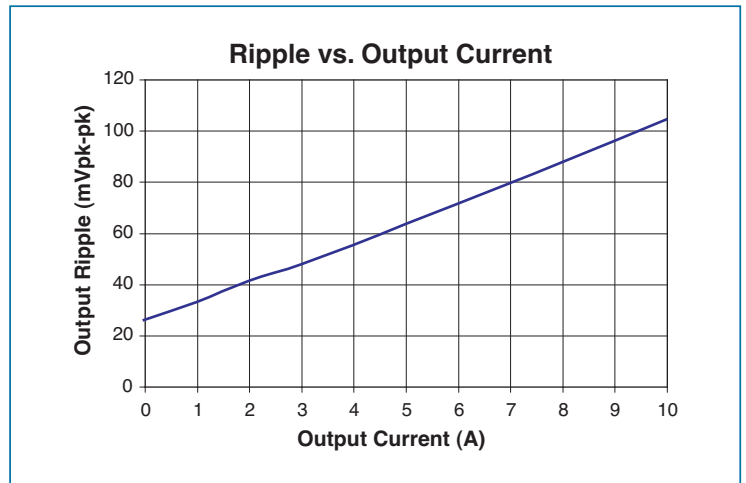


Figure 2 — Sample output voltage ripple vs. output current with no POL bypass capacitance. (MT036A120M010FP)

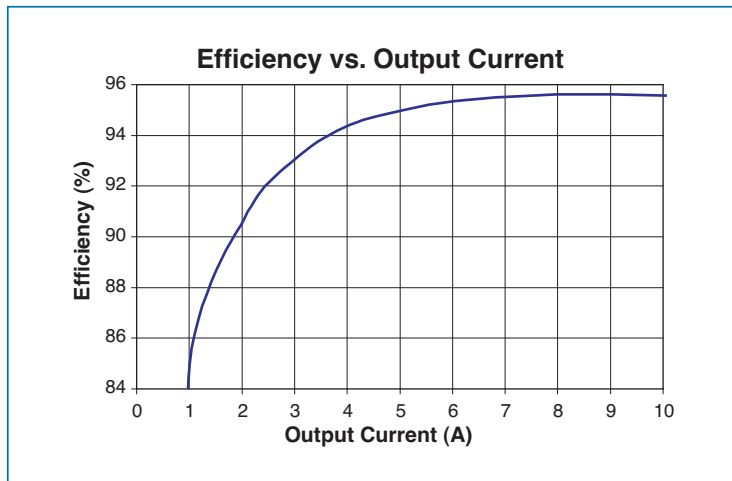


Figure 3 — Representative efficiency vs. output current. (MT036A120M010FP)

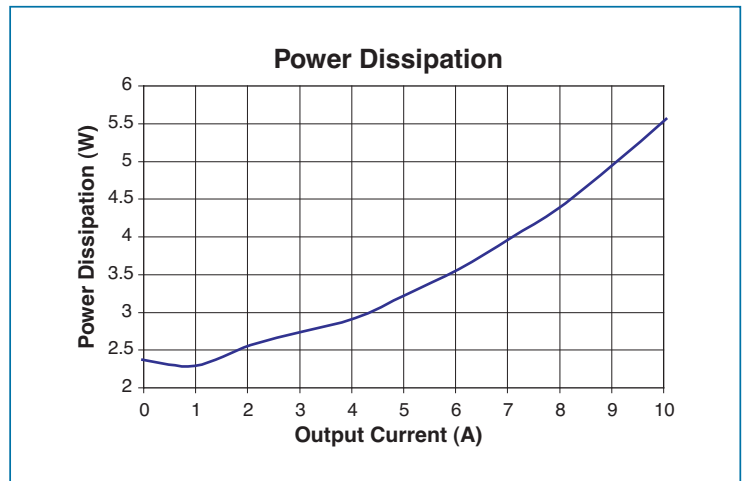


Figure 4 — Example power dissipation vs. output current. (MT036A120M010FP)

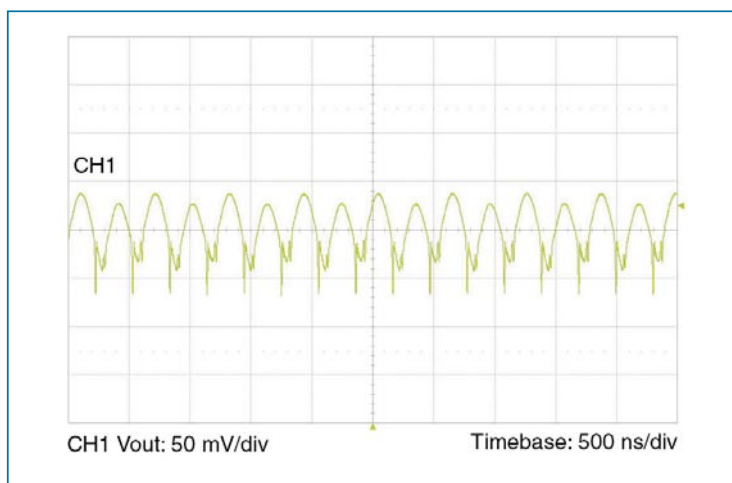


Figure 5 — Sample output voltage ripple at full load; with no POL bypass capacitance. (MT036A120M010FP)

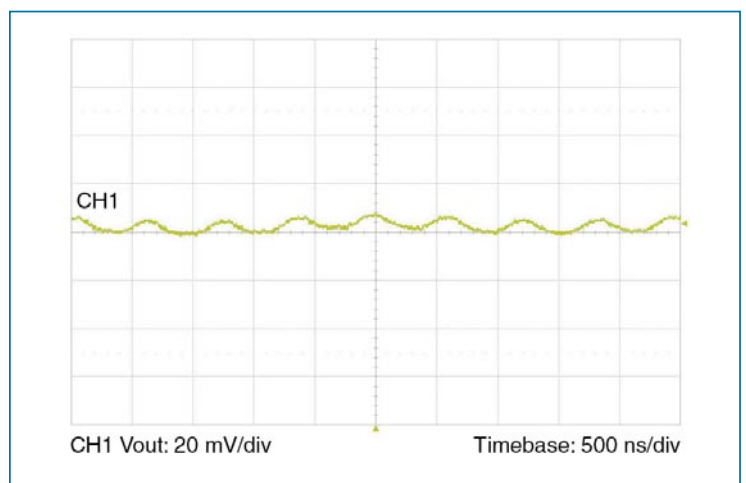


Figure 6 — Sample output voltage ripple at full load with 4.7  $\mu$ F ceramic POL bypass capacitance and 20 nH distribution inductance. (MT036A120M010FP)

TYPICAL WAVEFORMS

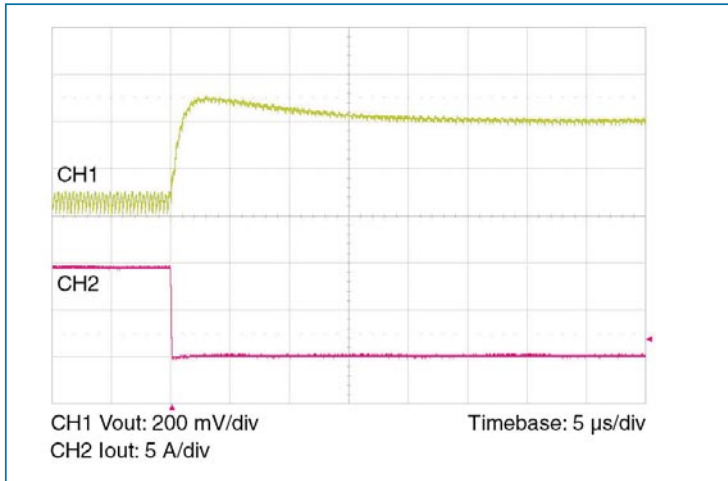


Figure 7 — Example load step with 100  $\mu$ F input capacitance and no output capacitance. (MT036A120M010FP)

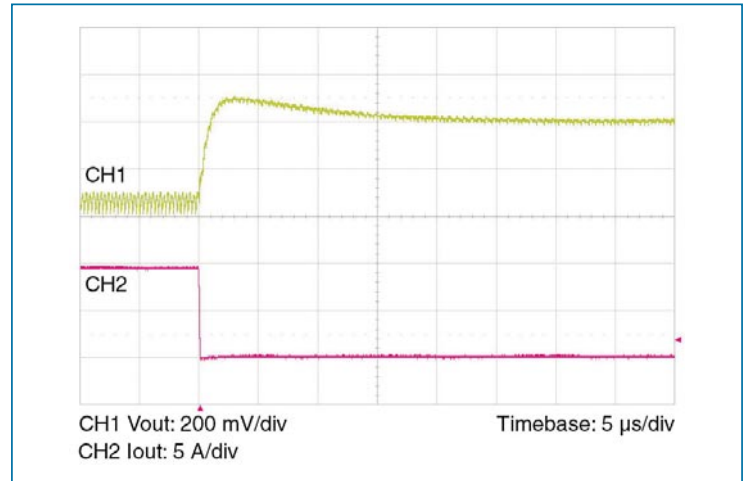


Figure 8 — Example load step with 100  $\mu$ F input capacitance and no output capacitance. (MT036A120M010FP)

## Military Cots VTM Family Part Numbers and Ranges

Part Number	K-Factor	Rated Output Current (A)	No Load Output Voltage (Vdc)		Rout (mΩ)		
			@26 Vin	@ 50 Vin	Min	Nom	Max
MT036A011M100FP	1/32	100	0.82	1.55	0.5	0.85	1.3
MT036A015M080FP	1/24	80	1.1	2.0	1.0	1.25	1.5
MT036A022M055FP	1/16	55	1.63	3.1	1.4	1.75	2.0
MT036A030M040FP	1/12	40	2.2	4.1	1.45	2.4	3.4
MT036A045M027FP	1/8	27	3.3	6.2	3.5	5.1	6.6
MT036A060M020FP	1/6	20	4.3	8.3	5.0	8.0	10
MT036A072M017FP	1/5	16.6	6.4 <sup>[a]</sup>	10	6.0	9.6	12
MT036A090M013FP	1/4	13.3	6.5	12.5	6.9	9.3	11.6
MT036A120M010FP	1/3	10.0	8.7	16.6	25	31	35
MT036A180M007FP	1/2	6.7	13	25	27.5	35.7	46.4
MT036A240M005FP	2/3	5.0	17.4	33	49.3	70.6	91.8
MT036A360M003FP	1	3.3	26	50	140	170	200

Table 1 — VTM part numbers

<sup>[a]</sup> Low line input voltage 32 V

Part Number	Typical Full Load Efficiency at nom Vout (%)	Typical Half Load Efficiency at nom Vout (%)	Maximum Load Capacitance (μF)
MT036A011M100FP	89.5	91.5	48128
MT036A015M080FP	92	94	27072
MT036A022M055FP	94	94.5	12032
MT036A030M040FP	94	95.0	6768
MT036A045M027FP	95.3	96.5	3008
MT036A060M020FP	95.3	96.8	1692
MT036A072M017FP	96.5	96.5	1175
MT036A090M013FP	96.3	95.5	752
MT036A120M010FP	95.5	95.5	423
MT036A180M007FP	96.0	95.2	188
MT036A240M005FP	95.0	94.8	106
MT036A360M003FP	96	96	47

Table 2 — Typical efficiency and maximum load capacitance, by part number

## Control Pin Functions

### VC – VTM Control

The VC port is multiplexed. It receives the initial V<sub>CC</sub> voltage from an upstream PRM, synchronizing the output rise of the VTM with the output rise of the PRM. Additionally, the VC port provides feedback to the PRM to compensate for the VTM output resistance. In typical applications using VTMs powered from PRMs, the PRM's VC port should be connected to the VTM VC port.

In applications where a VTM is being used without a PRM, 14 V must be supplied to the VC port for as long as the input voltage is below 26 V and for 10 ms after the input voltage has reached or exceeded 26 V. The VTM is not designed for extended operation below 26 V. The VC port should only be used to provide V<sub>CC</sub> voltage to the VTM during startup.

### PC – Primary Control

The Primary Control (PC) port is a multifunction port for controlling the VTM as follows:

**Disable** – If PC is left floating, the VTM output is enabled. To disable the output, the PC port must be pulled lower than 2.4 V, referenced to -In. Optocouplers, open collector transistors or relays can be used to control the PC port. Once disabled, 14 V must be re-applied to the VC port to restart the VTM.

**Primary Auxiliary Supply** – The PC port can source up to 2.4 mA at 5 Vdc.

## SPECIFICATIONS (CONT.)

### General Specifications

Parameter	Min	Typ	Max	Unit	Notes
MTBF (MT036A120M010FP)					
MIL-HDBK-217F		5,046,701		Hours	25°C, GB
		908,153			50°C NS
		711,584			65°C AIC
Isolation specifications					
Voltage	2,250			Vdc	Input to output
Capacitance		3,000		pF	Input to output
Resistance	10			MΩ	Input to output
<a href="#">Agency approvals</a>		cTÜVus			UL/CSA 60950-1, EN 60950-1
		CE Mark			Low voltage directive
Mechanical					
Weight		1.10/31.3		oz/g	See Mechanical Drawings, Figures 15, 16
Dimensions					
Length		1.91/48,6		in/mm	Baseplate model
Width		1.09/27,7		in/mm	Baseplate model
Height		0.37/9,5		in/mm	Baseplate model
Thermal					
Over temperature shutdown	125	130	135	°C	Junction temperature
Thermal capacity		23.8		Ws/°C	
Baseplate-to-ambient		7.7		°C/W	
Baseplate-to-ambient; 1000 LFM		2.9		°C/W	
Baseplate-to-sink; flat, greased surface		0.40		°C/W	
Baseplate-to-sink; thermal pad		0.36		°C/W	

### Auxiliary Pins

Parameter	Min	Typ	Max	Unit	Notes
Primary Control (PC)					
DC voltage	4.8	5.0	5.2	Vdc	
Module disable voltage	2.4	2.5		Vdc	
Module enable voltage		2.5	2.6	Vdc	VC voltage must be applied when module is enabled using PC
Current limit	2.4	2.5	2.9	mA	Source only
Disable delay time		10		μs	PC low to Vout low
VTM Control (VC)					
External boost voltage	12	6	19	Vdc	Required for VTM start up without PRM
External boost duration		10		ms	Vin > 26 Vdc. VC must be applied continuously if Vin < 26 Vdc.

### +In / -In DC Voltage Ports

The VTM input should not exceed the maximum specified. Be aware of this limit in applications where the VTM is being driven above its nominal output voltage. If less than 26 Vdc is present at the +In and -In ports, a continuous VC voltage must be applied for the VTM to process power. Otherwise VC voltage need only be applied for 10 ms after the voltage at the +In and -In ports has reached or exceeded 26 Vdc. If the input voltage exceeds the overvoltage turn-off, the VTM will shutdown. The VTM does not have internal input reverse polarity protection. Adding a properly sized diode in series with the positive input or a fused reverse-shunt diode will provide reverse polarity protection.

### TM – For Factory Use Only

### VC – VTM Control

The VC port is multiplexed. It receives the initial  $V_{CC}$  voltage from an upstream PRM, synchronizing the output rise of the VTM with the output rise of the PRM. Additionally, the VC port provides feedback to the PRM to compensate for the VTM output resistance. In typical applications using VTMs powered from PRMs, the PRM's VC port should be connected to the VTM VC port.

In applications where a VTM is being used without a PRM, 14 V must be supplied to the VC port for as long as the input voltage is below 26 V and for 10 ms after the input voltage has reached or exceeded 26 V. The VTM is not designed for extended operation below 26 V. The VC port should only be used to provide  $V_{CC}$  voltage to the VTM during startup.

### PC – Primary Control

The Primary Control (PC) port is a multifunction port for controlling the VTM as follows:

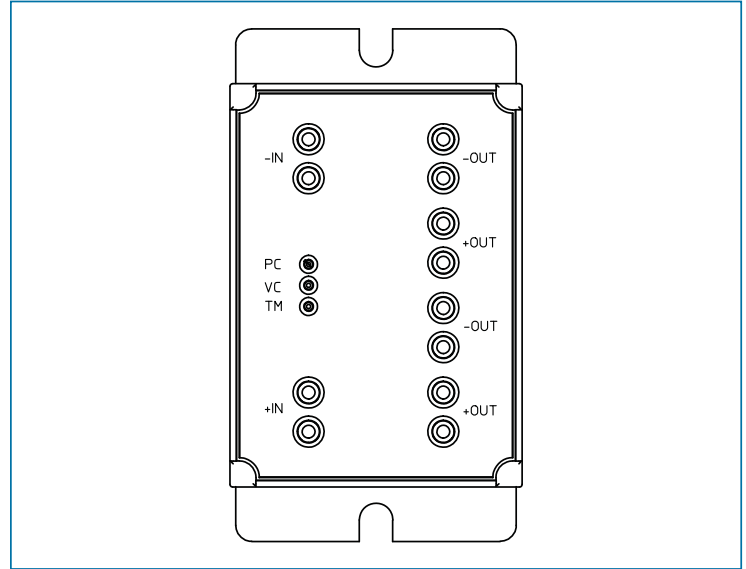
**Disable** – If PC is left floating, the VTM output is enabled. To disable the output, the PC port must be pulled lower than 2.4 V, referenced to -In. Optocouplers, open collector transistors or relays can be used to control the PC port. Once disabled, 14 V must be re-applied to the VC port to restart the VTM.

**Primary Auxiliary Supply** – The PC port can source up to 2.4 mA at 5 Vdc.

### +Out / -Out DC Voltage Output Ports

The output and output return are through two sets of contact locations. The respective +Out and -Out groups must be connected in parallel with as low an interconnect resistance as possible.

To take full advantage of the VTM, the user should note the low output impedance of the device. The low output impedance provides fast transient response without the need for bulk POL capacitance. Limited-life electrolytic capacitors required with conventional converters can be reduced or even eliminated, saving cost and valuable board real estate.



**Figure 9** — VI BRICK VTM pin configuration (viewed from pin side)

## Parallel Operation

In applications requiring higher current or redundancy, VTM's can be operated in parallel without adding control circuitry or signal lines. To maximize current sharing accuracy, it is imperative that the source and load impedance on each VTM in a parallel array be equal. If VTM's are being fed by an upstream PRM, the VC nodes of all VTM's must be connected to the PRM VC.

To achieve matched impedances, dedicated power planes within the PC board should be used for the output and output return paths to the array of paralleled VTM's. This technique is preferable to using traces of varying size and length.

The VTM power train and control architecture allow bi-directional power transfer when the VTM is operating within its specified ranges. Bi-directional power processing improves transient response in the event of an output load dump. The VTM may operate in reverse, returning output power back to the input source. It does so efficiently.

## Input Impedance Recommendations

To take full advantage of the VTM's capabilities, the impedance of the source (input source plus the PC board impedance) must be low over a range from DC to 5 MHz. The input of the VTM (factorized bus) should be locally bypassed with a 8  $\mu\text{F}$  low Q aluminum electrolytic capacitor. Additional input capacitance may be added to improve transient performance or compensate for high source impedance. The VTM has extremely wide bandwidth so the source response to transients is usually the limiting factor in overall output response of the VTM.

Anomalies in the response of the source will appear at the output of the VTM, multiplied by its K factor of 1/8. The DC resistance of the source should be kept as low as possible to minimize voltage deviations on the input to the VTM. If the VTM is going to be operating close to the high limit of its input range, make sure input voltage deviations will not trigger the input overvoltage turn-off threshold.

## Input Fuse Recommendations

VI BRICKs are not internally fused in order to provide flexibility in configuring power systems. However, input line fusing of VI BRICKs must always be incorporated within the power system. A fast acting fuse is required to meet safety agency Conditions of Acceptability. The input line fuse should be placed in series with the +In port. For agency approvals and fusing conditions, click on the link below:

[http://www.vicorpower.com/technical\\_library/technical\\_documentation/quality\\_and\\_certification/safety\\_approvals/](http://www.vicorpower.com/technical_library/technical_documentation/quality_and_certification/safety_approvals/)

## Application Notes

For VTM and VI BRICK application notes on soldering, thermal management, board layout, and system design click on the link below:

[http://www.vicorpower.com/technical\\_library/application\\_information/](http://www.vicorpower.com/technical_library/application_information/)

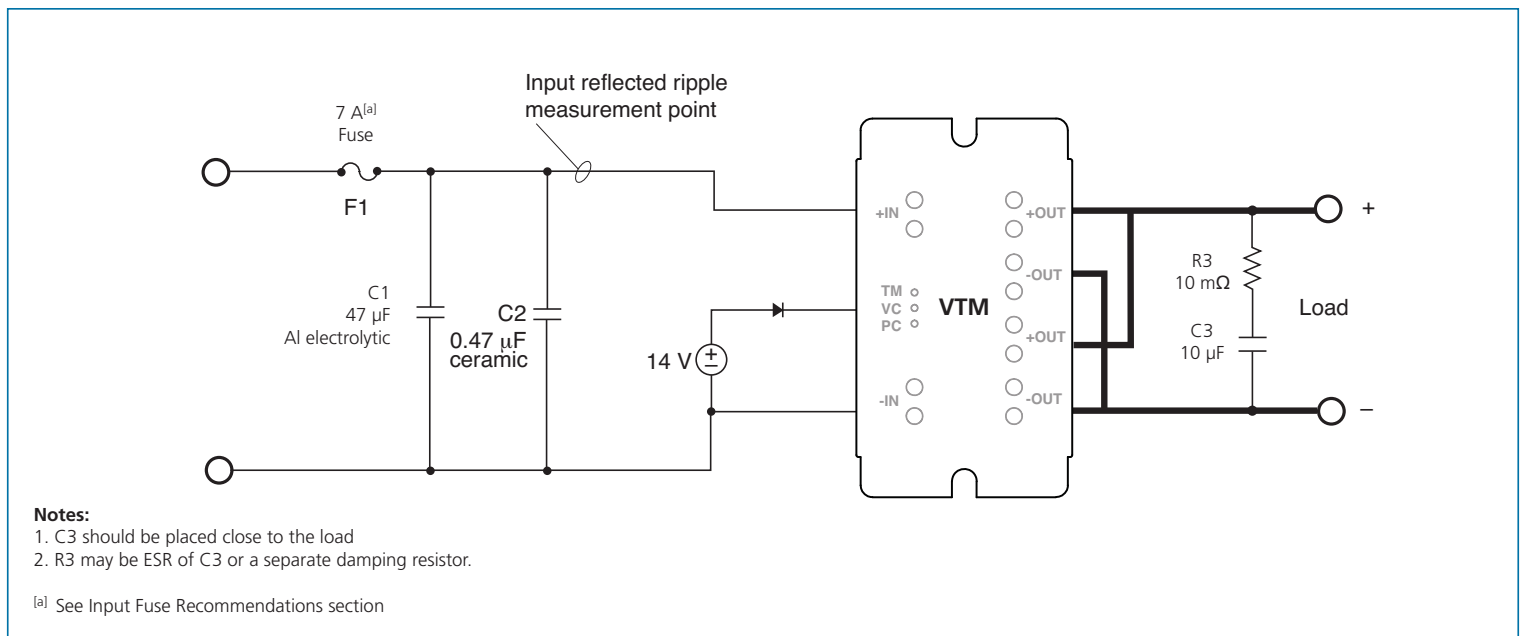


Figure 10 — VI BRICK VTM test circuit

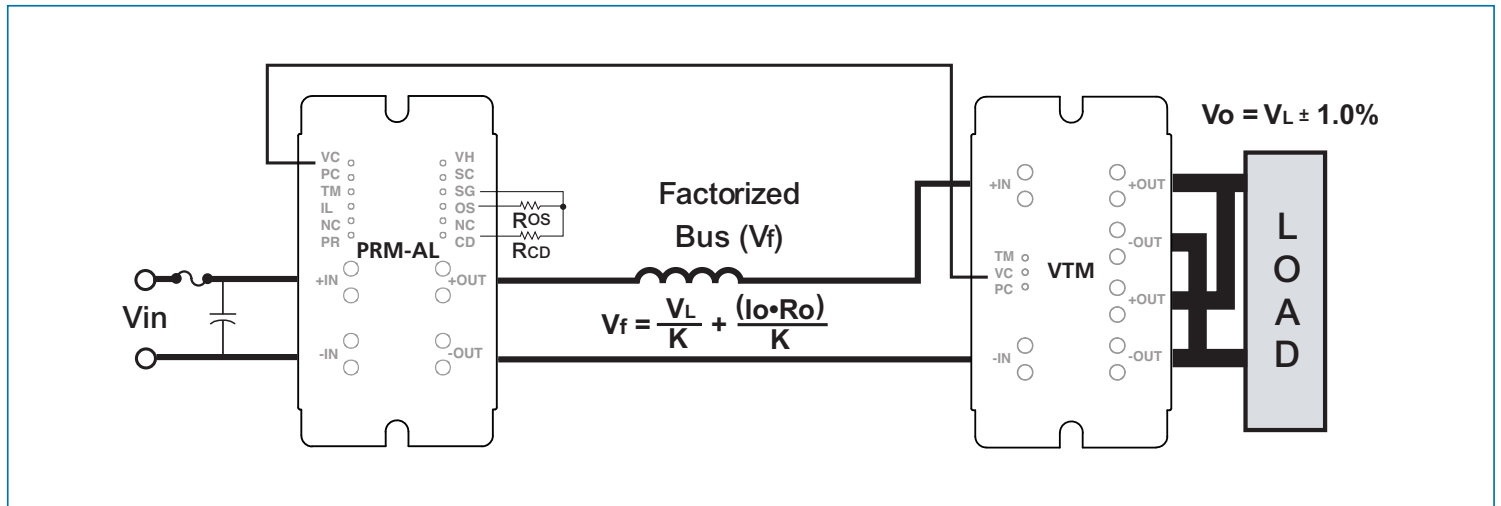
## APPLICATION NOTES (CONT.)

In figures below;

$K$  = VTM transformation ratio  
 $R_o$  = VTM output resistance

$V_f$  = PRM output (Factorized Bus Voltage)  
 $V_o$  = VTM output  
 $V_L$  = Desired load voltage

### FPA ADAPTIVE LOOP



**Figure 11** — The PRM controls the factorized bus voltage,  $V_f$ , in proportion to output current to compensate for the output resistance,  $R_o$ , of the VTM. The VTM output voltage is typically within 1% of the desired load voltage ( $V_L$ ) over all line and load conditions.

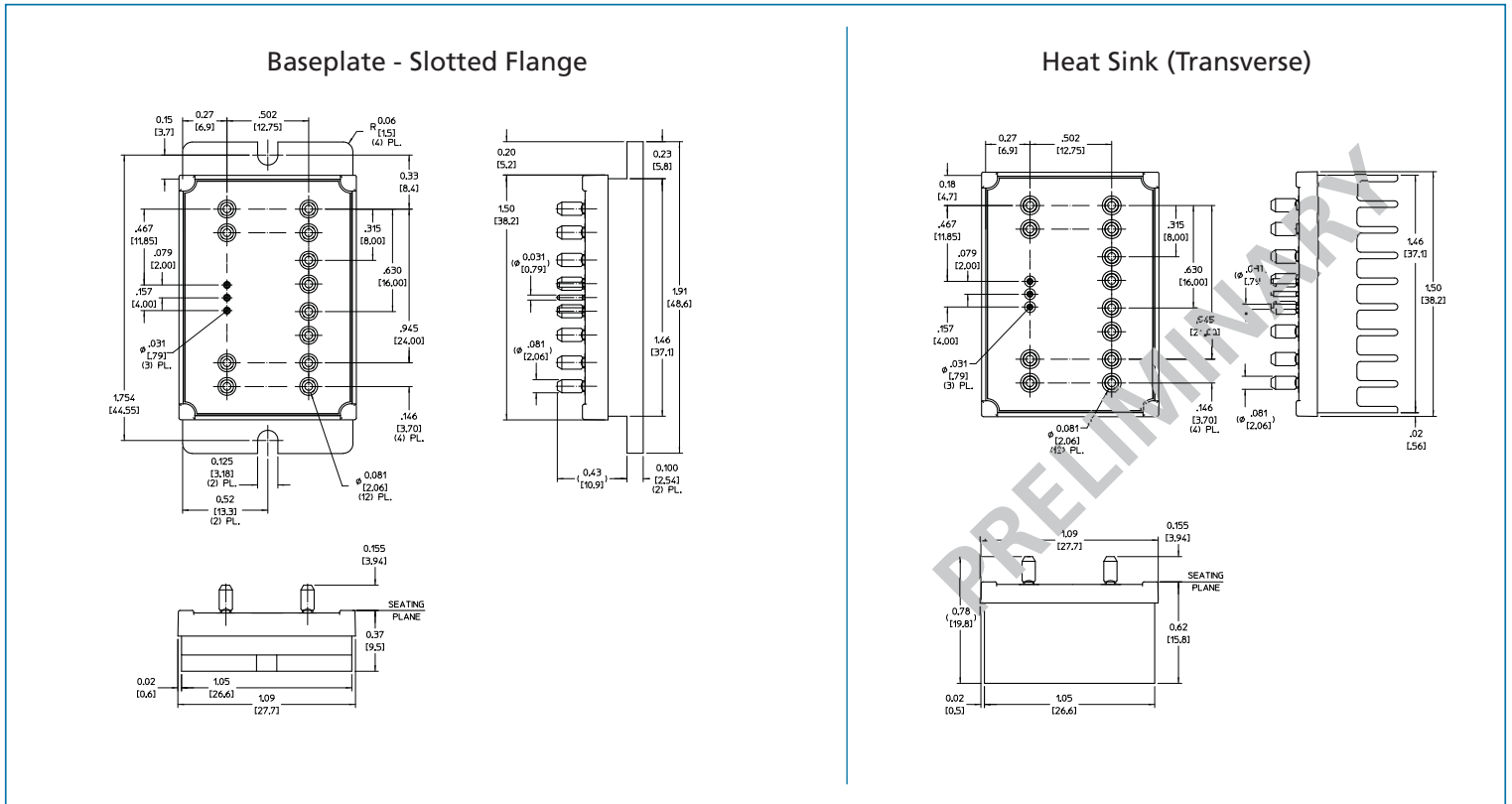


Figure 15 — Module outline

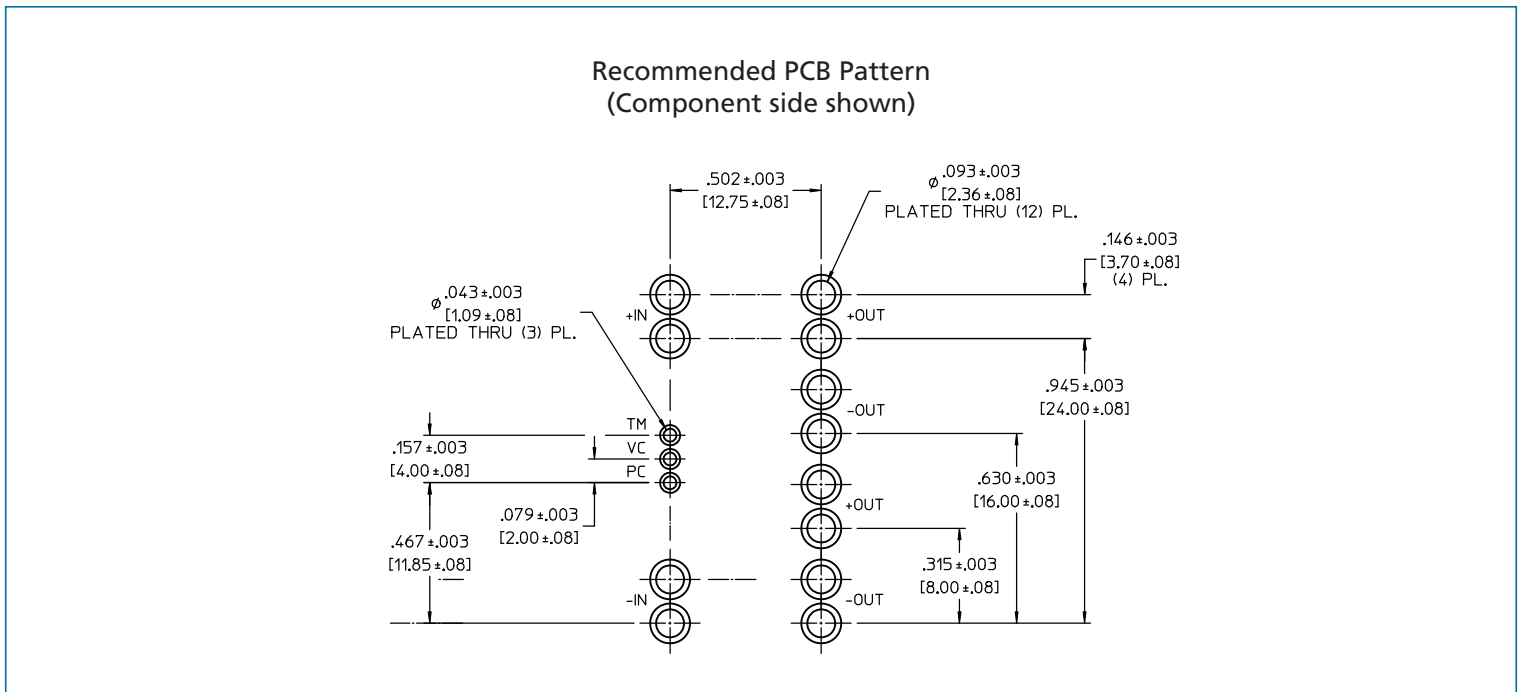


Figure 16 — PCB mounting specifications

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7,166,898; 7,187,263; D496,906; D505,114; D506,438; D509,472

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